# MODEL 256KMB-100 DYNAMIC RAM MEMORY BOARD 



## FEATURES

IEEE S100 BUS Compliance 262,144 Byte ( 256 Kbyte) capacity

- 225 Nano-second access time (max); 160 NS (typ) 295 Nano-second read/write time (min)
- Bank selectable; divisible into 16 banks each 16384 bytes (16 Kbytes) in size. Options provided to combine banks into 4-64 Kbyte banks, 8-32 Kbyte banks, 16-16 Kbyte banks or any combination of 16 Kbyte banks.
- I/O Port Address Bank Selection.
- Configurable for up to 2 Megabytes of contiguous memory on 64 Kbyte boundaries.
- Deselective from 4 Kbytes to 64 Kbytes on 4 Kbyte boundaries.
- Configurable for Phantom deselection.
- Parity Error Detection (visual and/or through interrupts)
- Jumper Options provided to accommodate IEEE/ 8080/Z80/ALPHA-MICRO timing.
- Bank Selection Scheme Compatible wizh CROMIXтм, CP/M 2.2 ${ }^{\text {™ }}, \mathrm{MP} / \mathrm{M}^{\text {™ }}$, ALPHA-MICRO \& other major systems.
- Fully compatible with the ICM CPZ-48000 Single Board Central Processor.


## DESCRIPTION

The $256 \mathrm{KMB}^{\text {™ }}$ Dynamic Ram memory board is an S100BUS/IEEE 696.1 compatible board accommodating 262,144 bytes ( 256 Kbyte) of read/write memory. The 256 KMB $^{\text {тм }}$ incorporates the $4164 \mathrm{~S}-15064 \mathrm{~K} \times 1$ bit dynamic RAM chip jiving the user 225 nano-second (max) access time with simple, reliable $\mathrm{Z80}$ or 8080 refresh capability. The board may be operated as a BANK SELECTABLE or LINEAR ADDRESSABLE memory.

BANK SELECTION: Up to 16 independently addressable banks of 16 Kbytes may be configured in the BANK SELECTION scheme.

Each bank may reside at addresses within a 64 Kbyte address space starting at location $0000 \mathrm{H}, 4000 \mathrm{H}, 8000 \mathrm{H}$ or C 000 H as set by jumper options. One or more banks may reside in the same address space. Each bank is individually enabled or disabled at system reset time, depending on jumper option settings. Each bank is selectable through open collector data BUS drivers via 20 pin dip headers to allow complete flexibility in implementing bank selection methods compatible with CROMEMCO (opencollector OR-ties to select banks simultaneously) or ALPHAMICRO/NORTH STAR (banks selected in direct correspondance with active data bits). Each bank may be "phantomed" (disabled when the S100 BUS signal PHANTOM goes active) or may be configured to disregard phantom.

LINEAR ADDRESSING: Up to 2 megabytes of linear address memory may be configured. The beginning address may commence at any 64 Kbyte boundary as specified by the user.

OTHER FEATURES: A window of deselection within the 64 Kbyte address space may be specified via headers. The window may take any size from 4 K to 64 Kbytes and may reside at 4 Kbyte boundaries. The starting and ending address of deselection are specified through headers. Parity error detection is provided. A light emitting diode gives visual error indications and the user may connect the error signal to MNI (Pin 12) or ERROR (Pin 98) of the S100 BUS. Refresh is accomplished with minimal circuitry thus providing greater reliability. The $\mathbf{2 5 6 K M B}$ тм is ideal for operation as a turbo disk file cache also known as "Memory disk". Operating the CPZ48000 Central Processor Unit with TURBODISK ${ }^{\text {TM }}$ and memory-to-memory transfers under direct memory access (DMA) control, block move transfers are enhanced by a factor of 3 over Z80™ $^{\text {¹ }}$ block moves.


1733 South Douglass Road, Suite E• Anaheim, California 92806

# PERFORMANCE SPECIFICATIONS MODEL 256KMB-100 DYNAMIC RAM MEMORY BOARD 

BUS INTERFACE IEEE 696.1/D2
MICROPROCESSOR COMPATIBILITY Any Z80 or 8080 board micro processoroperating up to 4 MHz
WAIT STATES ..... None required
MEMORY CAPACITY 262,144 bytes (256 Kbytes)
MEMORY ACCESS TIME . 225 Nano-seconds (max)
READ/WRITE CYCLE TIME 295 Nano-seconds (min)
BANK SELECTION . ...................................................................... Banks set or reset through I/O Port Commands.I/O Port Address Assignmentselectable through jumper options
 or any combinatin of 16 Kby Kant信 5-48 Kbyte banks and 1-16 Kbyte bank
$\qquad$
Phantom ....... or disabled through jumper options

. All banks disbled with PHANTOM or configured to disregard PHANTOI
with jumper option
Address Allocation. Each bank assignable to location 0000 H ,$4000 \mathrm{H}, 8000 \mathrm{H}$, or C 000 H through jumper options.
I/O Port Assignments A7 A6 A5 A4 A3 A2 A1 A0 Function ..... $x \times x \times x \times 0$ o Bank Select OH-7H $x \quad x \quad x \quad x \quad x \quad x \quad o \quad 1 \quad$ Bank Select $8 \mathrm{H}-\mathrm{FH}$ $x \quad x \quad x \quad x \quad x \quad x \quad 1 \quad o \quad$ Clear Parity Error $x \quad x \quad x \quad x \quad x \quad x \quad 1 \quad 1$ Undefined
a contiguous memory spanning an address of 000000 H to1FFFFFH for a total of 2,097, 152 bytes (2 Megabytes)
WINDOW DESELECTION 4 K to 64 Kbytes of deselection on 4 Kybte boundaries
POWER REQUIREMENTS
Voltages. +8 V DC @ 1.5 A (max)
Power. 12W (max)
OPERATING ENVIRONMENT
Temperature0 to 45 Degrees Celsius
Relative Humidity 0 to $95 \%$
CONSTRUCTION
Circuit Board

